ABSTRACT OF THE DISCLOSURE

[0061] The present invention provides a turbo-code decoder that adopts the parallel and systolic array VLSI structure design. Since the output of previous level can be used as the input of next level. So the advantages of the parallel and the pipeline calculation are totally achieved. The latency is only N+M+2 units of time, the latency is shorten to as about 1/5 comparing to the conventional sequential calculation structure that takes 5*(N+M) units of time. The decoding throughput is about 5*(N+M) times higher than the conventional decoder. Although the quantity of the circuit gate is about 5*(N+M) times higher than the conventional decoder. However, the VLSI techniques had been progressively improved nowadays, thus the hardware complexity is easy to overcome. Devoting the hardware cost to get the higher speed will be a changeless trend.